Claim Amendments

Please amend claims 1, 4, and 11 as follows:

Please cancel claim 5 as follows:

Please add new claim 21 as follows:

Listing of Claims

What is claimed is:

1. (currently amended) A method for forming triple polysilicon split gate electrodes in an EEPROM flash memory array comprising the steps of:

providing a ~~first~~ gate structure comprising a gate dielectric formed over a semiconductor substrate, an overlying first polysilicon electrode and an overlying first dielectric insulating layer;

~~blanket depositing~~ forming a first polysilicon layer over the ~~first~~ gate structure;

etching back the first polysilicon layer through a portion of the first polysilicon layer thickness according to a first dry etching process to partially smooth the first polysilicon layer topography;

~~blanket depositing~~ forming a second dielectric insulating layer over the first polysilicon layer;

~~blanket depositing~~ forming a second polysilicon layer over the second dielectric insulating layer; and,

then lithographically patterning and dry etching according to [[a]] respective ~~third and fourth~~ sequential dry etching processes through a thickness portion of the respective second and first polysilicon layers to respectively form third and second polysilicon gate electrodes.

2. (original) The method of claim 1, wherein at least the first dry etching process comprises a downstream chemically dependent etching (CDE) process.

3. (original) The method of claim 1, wherein the first polysilicon layer is deposited to a thickness greater by a factor of about 1 to about 2.5 compared to a final thickness following the step of etching back.

4. (currently amended) The method of claim 1, following the step of etching back and prior to the step of ~~blanket depositing~~ forming a second dielectric insulating layer, further comprising the steps of:

~~blanket depositing~~ forming a dielectric anti-reflectance coating (DARC) layer over the first polysilicon layer; and,

lithographically patterning and etching according to a second dry etching process through a thickness portion of the first polysilicon layer[[;]].

5. cancelled.

6. (original) The method of claim 1, wherein the first polysilicon gate electrode comprises a select gate, the second polysilicon gate electrode comprises a floating gate and the third polysilicon gate electrode comprises a control gate.

7. (original) The method of claim 1, wherein the first and second dielectric insulating layers are selected from the group consisting of thermally grown silicon oxide and sequential layers of silicon oxide/silicon nitride/silicon oxide.

8. (original) The method of claim 1, wherein the first dielectric insulating layer comprises thermally grown silicon oxide.

9. (original) The method of claim 1, wherein the second

dielectric insulating layer comprises sequential layers of silicon oxide/silicon nitride/silicon oxide (ONO).

10. (original) The method of claim 1, wherein the third polysilicon gate electrode is formed comprising a first edge aligned with an underlying edge of the second polysilicon gate electrode which is aligned over a portion of the first polysilicon gate electrode.

11. (currently amended) The method of claim 1, wherein the ~~fourth~~ sequential dry etching processes comprises a downstream chemically dependent etching (CDE) process.

12. (original) The method of claim 1, wherein at least the second dry etching process comprises forming one of rows and columns of active areas in a memory cell matrix.

13. (original) A polysilicon etching process for forming triple polysilicon split gate electrodes in an EEPROM flash memory array with improved electrical properties and reduced dry etching residues comprising the steps of:

providing a first polysilicon select gate structure comprising a gate oxide formed over a semiconductor substrate, an overlying polysilicon select gate electrode, an overlying first insulating interpoly layer, dielectric sidewall spacers, and a tunnel oxide layer formed adjacent the first polysilicon gate structure and overlying the semiconductor substrate;

blanket depositing a first polysilicon layer over the first polysilicon select gate structure;

etching back the first polysilicon layer through a thickness portion according to a first dry etching process;

blanket depositing a dielectric anti-reflectance coating (DARC) layer over the first polysilicon layer;

lithographically patterning and etching according to a second dry etching process a portion of the first polysilicon layer to form active areas;

blanket depositing a second insulating interpoly layer over the first polysilicon layer;

blanket depositing a second polysilicon layer over the second interpoly layer; and, lithographically patterning and dry etching according to a third dry etching process through a thickness portion of the second polysilicon layer to stop on the second insulating interpoly layer to form a polysilicon control gate.

14. (original) The method of claim 13, further comprising the step of dry etching according to a fourth dry etching process through the second insulating interpoly layer and a thickness portion of the first polysilicon layer to form a polysilicon floating gate.

15. (original) The method of claim 14, wherein the polysilicon floating gate is aligned over a portion of the polysilicon select gate and self-aligned with the overlying polysilicon control gate.

16. (original) The method of claim 13, wherein at least the first dry etching process comprises a downstream chemically dependent etching (CDE) process.

17. (original) The method of claim 13, wherein the first polysilicon layer is deposited to a thickness greater by a factor

of about 1 to about 2.5 compared to a final thickness following the step of etching back.

18. (original) The method of claim 13, wherein the DARC layer is deposited to a thickness between about 500 Angstroms and about 1500 Angstroms.

19. (original) The method of claim 13, wherein the first insulating interpoly layer comprises thermally grown silicon oxide.

20. (original) The method of claim 12, wherein the second insulating interpoly layer comprises sequential layers of silicon oxide/silicon nitride/silicon oxide (ONO).

21. (new) A method for forming triple polysilicon split gate electrodes in an EEPROM flash memory array comprising the steps of:

providing a first gate structure comprising a gate dielectric formed over a semiconductor substrate, an overlying first polysilicon electrode and an overlying first dielectric insulating layer;

forming a first polysilicon layer over the first gate structure;

etching back the first polysilicon layer according to a first dry etching process;

forming a dielectric anti-reflectance coating (DARC) layer over the first polysilicon layer;

lithographically patterning and etching according to a second dry etching process through a thickness portion of the first polysilicon layer;

forming a second dielectric insulating layer over the first polysilicon layer;

forming a second polysilicon layer over the second dielectric insulating layer; and,

lithographically patterning and dry etching according to a respective third and fourth dry etching process through a thickness portion of the respective second and first polysilicon layers to respectively form third and second polysilicon gate electrodes.